HERMETIC PACKAGES AND FEEDTHROUGHS FOR NEURAL PROSTHESES

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SUMMARY

During the past quarter progress was made in a number of areas related to in-vitro and in-vivo testing of glass-Si packages, testing of electroplated gold coatings, and redesign of the circuit blocks for a fully-integrated nerve stimulation system (FINESS).

A wireless system that consists of a hybrid coil and a polyimide relative humidity sensor has been developed. We have packaged a wireless system and soaked it in high temperature saline and after 21 months in saline at 97°C, the humidity monitoring system is functional and the package is still dry (confirmed with visual inspection). Six glass-silicon packages with HMS systems have been explanted from the two guinea pigs and all humidity sensors indicate that the packages remained hermetic and intact. IHS devices have been fabricated and various tests completed. The test results suggest that the IHS works well and can be effectively utilized in future packaging technologies. A paper entitled "A Passive Wireless Integrated Humidity Sensor" has been accepted for journal publication in Sensors and Actuators special edition covering MEMS 2001.

We have expanded our research into electroplated gold films for hermetic packaging. We have made changes to the package design and to the test setup used to extract the MTTF. This new technique should allow us to make improved lifetime predictions. This technology is also in the process of being turned over to the neural recordings group for use in in-vivo studies.

Finally, the FINESS chip has been redesigned and optimized for operation under changing conditions. The original chip, designed about 3 years ago, had a narrow operation window. During the past quarter the entire chip was redesigned and layed out. The layout has been sent out for masks and fabrication will start in the coming quarter.

I. INTRODUCTION

This project aims at the development of hermetic, biocompatible micropackages and feedthroughs for use in a variety of implantable neural prostheses for sensory and motor handicapped individuals. In addition, it will also develop a telemetry system for monitoring package humidity in unrestrained animals, and of telemetry electronics and packaging for stimulation of peripheral nerves. The primary objectives of the proposed research are: 1) the development and characterization of hermetic packages for miniature, silicon-based, implantable neural prostheses designed to interface with the nervous system for many decades; 2) the development of techniques for providing multiple sealed feedthroughs for the hermetic package; 3) the development of custom-designed packages and systems used in several different chronic stimulation or recording applications in the central or peripheral nervous systems in collaboration and cooperation with groups actively involved in developing such systems; and 4) establishing the functionality and biocompatibility of these custom-designed packages in *in-vivo* applications. Although the proposed research is focused on the development of the package and feedthroughs, it also aims at the development of inductively powered systems that can be used in many implantable recording and stimulation devices in general, and of multichannel microstimulators for functional neuromuscular stimulation, and multichannel recording microprobes for CNS applications in particular.

Our group here at the Center for Wireless Integrated Microsystems at the University of Michigan has been involved in the development of silicon-based multichannel recording and stimulating microprobes for use in the central and peripheral nervous systems. More specifically, during the past three contract periods dealing with the development of a single-channel inductively powered microstimulator, our research and development program has made considerable progress in a number of areas related to the above goals. A hermetic packaging technique based on electrostatic bonding of a custom-made glass capsule and a supporting silicon substrate has been developed and has been shown to be hermetic for a period of at least a few decades in salt water environments. This technique allows the transfer of multiple interconnect leads between electronic circuitry and hybrid components located in the sealed interior of the capsule and electrodes located outside of the capsule. The glass capsule can be fabricated using a variety of materials and can be made to have arbitrary dimensions as small as 1.8mm in diameter. A multiple sealed feedthrough technology has been developed that allows the transfer of electrical signals through polysilicon conductor lines located on a silicon support substrate. Many feedthroughs can be fabricated in a small area. The packaging and feedthrough techniques utilize biocompatible materials and can be integrated with a variety of micromachined silicon structures.

The general requirements of the hermetic packages and feedthroughs to be developed under this project are summarized in Table 1. Under this project we will concentrate our efforts to satisfy these requirements and to achieve the goals outlined above. There are a variety of neural prostheses used in different applications, each having different requirements for the package, the feedthroughs, and the particular system application. The overall goal of the program is to develop a miniature hermetic package that can seal a variety of electronic components such as capacitors and coils, and integrated circuits and sensors (in particular electrodes) used in neural prostheses. Although the applications are different, it is possible to identify a number of common requirements in all of these applications in addition to those requirements listed in Table 1. The packaging and feedthrough technology should be capable of:

1- protecting non-planar electronic components such as capacitors and coils, which typically have large dimensions of about a few millimeters, without damaging them;
2- protecting circuit chips that are either integrated monolithically or attached in a hybrid fashion with the substrate that supports the sensors used in the implant;
3- interfacing with structures that contain either thin-film silicon microelectrodes or conventional microelectrodes that are attached to the structure;

Table 1: General Requirements for Miniature Hermetic Packages and Feedthroughs for Neural Prostheses Applications.

Package Lifetime:

≥ 40 Years in Biological Environments @ 37°C

Packaging Temperature:

£360°C

Package Volume:

10-100 cubic millimeters

Package Material:

Biocompatible
Transparent to Light
Transparent to RF Signals

Package Technology:

Batch Manufactureable

Package Testability:

Capable of Remote Monitoring
In-Situ Sensors (Humidity & Others)

Feedthroughs:

At Least 12 with £125µm Pitch
Compatible with Integrated or Hybrid Microelectrodes
Sealed Against Leakage

Testing Protocols:

In-Vitro Under Accelerated Conditions
In-Vivo in Chronic Recording/Stimulation Applications

We have identified two general categories of packages that need to be developed for implantable neural prostheses. The first deals with those systems that contain large components like capacitors, coils, and perhaps hybrid integrated circuit chips. The second deals with those systems that contain only integrated circuit chips that are either integrated in the substrate or are attached in a hybrid fashion to the system.

Figure 1 shows our general proposed approach for the package required in the first category. This figure shows top and cross-sectional views of our proposed approach here. The package is a glass capsule that is electrostatically sealed to a support silicon substrate. Inside the glass capsule are housed all of the necessary components for the system. The electronic circuitry needed for any analog or digital circuit functions is either fabricated on a separate circuit chip that is hybrid mounted on the silicon substrate and electrically connected to the silicon substrate, or integrated monolithically in the support silicon substrate itself. The attachment of the hybrid IC chip to the silicon substrate can be performed using a number of different technologies such as simple wire bonding between pads located on each substrate, or using more sophisticated techniques such as flip-chip solder reflow or tab bonding. The larger capacitor or microcoil components are mounted on either the substrate or the IC chip using appropriate epoxies or solders. This completes the assembly of the electronic components of the system and it should be possible to test the system electronically at this point before the package is completed. After testing, the system is packaged by placing the glass capsule over the entire system and bonding it to the silicon substrate using an electrostatic sealing process. The cavity inside the glass package is now hermetically sealed against the outside environment. Feedthroughs to the outside world are provided using the grid-feedthrough technique discussed in previous reports. These feedthroughs transfer the electrical signals between the electronics inside the package and various elements outside of the package. If the package has to interface with conventional microelectrodes, these microelectrodes can be attached to bonding pads located outside of the package; the bond junctions will have to be protected from the external environment using various polymeric encapsulants. If the package has to interface with on-chip electrodes, it can do so by integrating the electrode on the silicon support substrate. Interconnection is simply achieved using on-chip polysilicon conductors that make the feedthroughs themselves. If the package has to interface with remotely located recording or stimulating electrodes that are attached to the package using a silicon ribbon cable, it can do so by integrating the cable and the electrodes again with the silicon support substrate that houses the package and the electronic components within it.

Figure 2 shows our proposed approach to package development for the second category of applications. In these applications, there are no large components such as capacitors and coils. The only component that needs to be hermetically protected is the electronic circuitry. This circuitry is either monolithically fabricated in the silicon substrate that supports the electrodes (similar to the active multichannel probes being developed by the Michigan group), or is hybrid attached to the silicon substrate that supports the electrodes (like the passive probes being developed by the Michigan group). In both of these cases the package is again another glass capsule that is electrostatically sealed to the silicon substrate. Notice that in this case, the glass package need not be a high profile capsule, but rather it need only have a cavity that is deep enough to allow for the silicon chip to reside within it. Note that although the silicon IC chip is originally 500μm thick, it can be thinned down to about 100μm, or can be recessed in a cavity created in the silicon substrate itself. In either case, the recess in the glass is less than 100μm deep (as opposed to several millimeters for the glass capsule). Such a glass package can be easily fabricated in a batch process from a larger glass wafer.

The above two approaches address the needs for most implantable neural prostheses. Note that both of these techniques utilize a silicon substrate as the supporting base, and are not directly applicable to structures that use other materials such as ceramics or metals. Although this may seem a limitation at first, we believe that the use of silicon is, in fact, an advantage because it is biocompatible and many emerging systems use silicon as a support substrate.

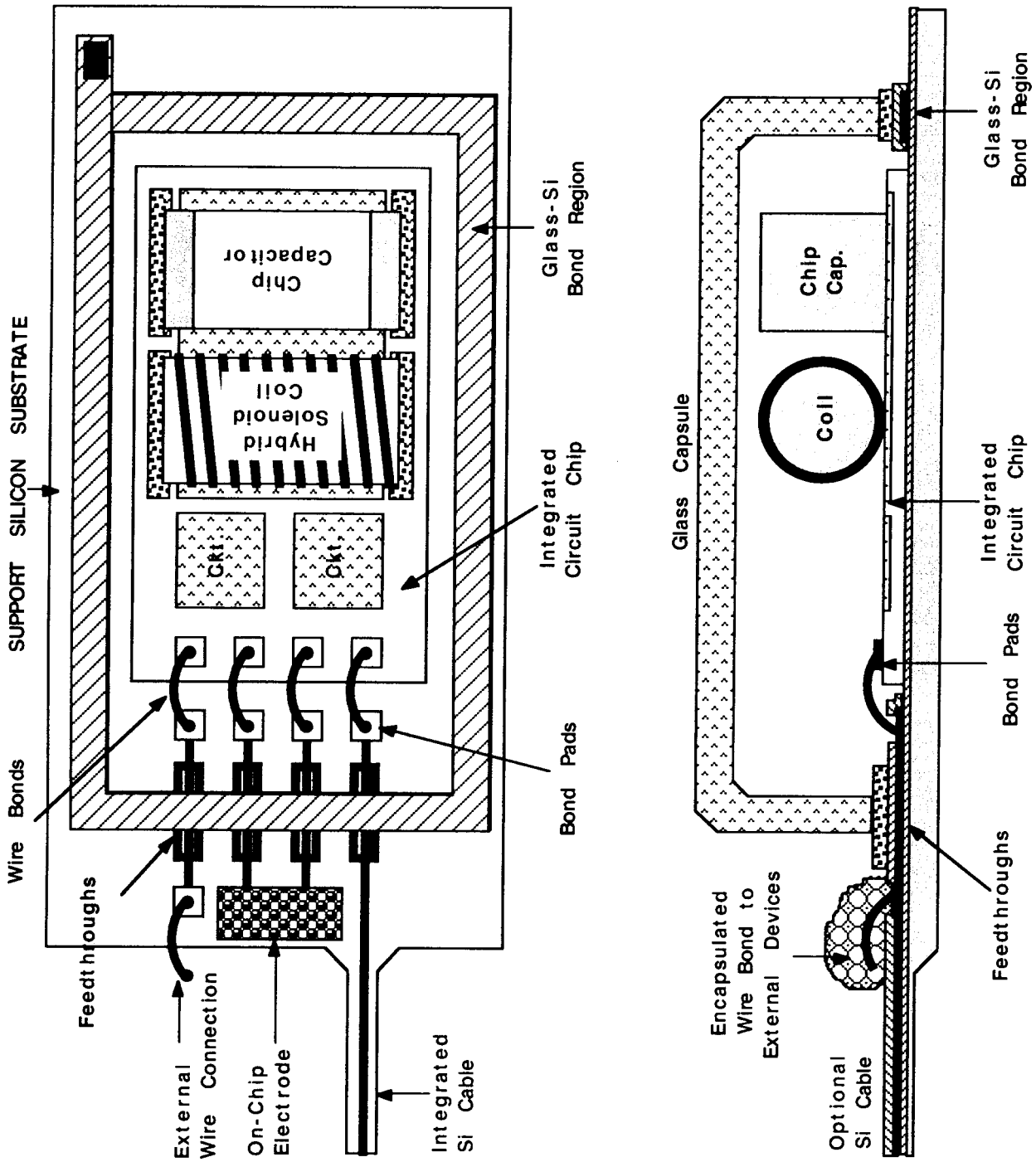

Figure 1: A generic approach for packaging implantable neural prostheses that contain a variety of components such as chip capacitors, microcoils, and integrated circuit chips. This packaging approach allows for connecting to a variety of electrodes.

We will further improve the silicon glass package and its built-in feedthroughs, and will study and explore alternative technologies for hermetic packaging of implantable systems. In particular, we have proposed using a silicon capsule that can be electrostatically bonded to a silicon substrate thus allowing the capsule to be machined down to dimensions below a 100μm. We will also develop an implantable telemetry system for monitoring package humidity in unrestrained animals for a period of at least one year. Two separate systems have been proposed, one based on a simple oscillator, and the other based on a switched-capacitor readout interface circuit and an on-chip low-power AD converter, both using a polyimide-based humidity sensor. This second system will telemeter the humidity information to an outside receiver using a 300MHz on-chip transmitter.

Finally, we have forged potential collaborations with two groups working in the development of recording/stimulating systems for neural prostheses. The first group is that led by Professor Ken Wise at the University of Michigan, which has been involved in the development of miniature, silicon-based multichannel recording and stimulation system for the CNS for many years. Through this collaboration we intend to develop hermetic packages and feedthroughs for a 3-D recording/stimulation system that is under development at Michigan. We will also develop the telemetry front end necessary to deliver power and data to this system. The second group is at Case Western Reserve University, led by Prof. D. Durand, and has been involved in recording and stimulation from peripheral nerves using cuff electrodes. Through this collaboration we intend to develop a fully integrated, low profile, multichannel, hermetic, wireless peripheral nerve stimulator that can be used with their nerve cuff electrode. This system can be directly used with other nerve cuffs that a number of other groups around the country have developed. Both of these collaborations should provide us with significant data on the reliability and biocompatibility of the package.

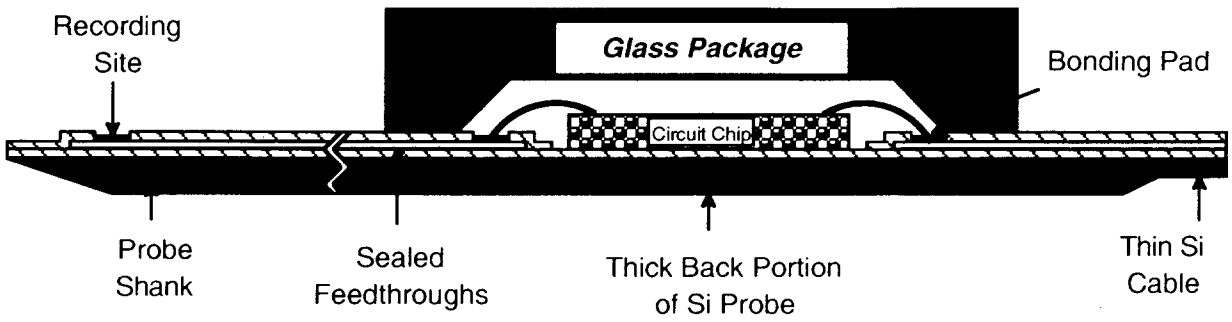

Figure 2: Proposed packaging approach for implantable neural prostheses that contain electronic circuitry, either monolithically fabricated in the probe substrate or hybrid attached to the silicon substrate containing microelectrodes.

II. ACTIVITIES DURING THE PAST QUARTER

2.1 Hermetic Packaging

Over the past few years we have developed a biocompatible hermetic package with high density multiple feedthroughs. This technology utilizes electrostatic bonding of a custom-made glass capsule to a silicon substrate to form a hermetically sealed cavity, as shown in Figure 3. Feedthrough lines are obtained by forming closely spaced polysilicon lines and planarizing them with LTO and PSG. The PSG is reflowed in steam at 1100°C for 2 hours to form a planarized surface. A passivation layer of oxide/nitride/oxide is then deposited on top to prevent direct exposure of PSG to moisture. A layer of fine-grain polysilicon (surface roughness 50Å rms) is deposited and doped to act as the bonding surface. Finally, a glass capsule is bonded to this top polysilicon layer by applying a voltage of 2000V between the two for 12 minutes at 320 to 350°C, a temperature compatible with most hybrid components. The glass capsule can be either custom molded from Corning code #7740 glass, or can be batch fabricated using ultrasonic micromachining of #7740 glass wafers.

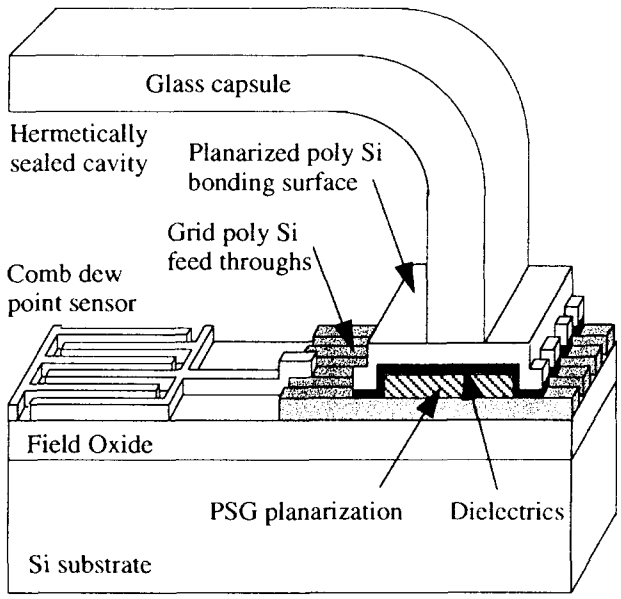

Figure 3: The structure of the hermetic package with grid feedthroughs.

During the past few years we have electrostatically bonded and soak tested over one hundred and sixty of these packages. The bonding yield is about 82% (yield is defined as the percentage of packages which last more than 24 hours in the solution they are soaked in). At the beginning of this quarter, 4 devices were still being tested in saline at room temperature. These devices have been under test for nearly 6.5 years and show no sign of leakage. We should mention that these devices have been made with silicon substrates that are thinned (~150μm) and bonded to the custom molded glass capsules. We have also continued fabrication of silicon

substrates and also continued several in-vivo and in-vitro tests using a wireless humidity sensor-hybrid coil system.

2.1.1 Room Temperature Soak Tests in Saline

The packages soaked in phosphate buffered saline at room temperature have been under test for over 6 years. These soak tests were started to complement the accelerated soak tests at the higher temperatures. Furthermore, upon close inspection of the top polysilicon layer, it is found that this top layer is there and is not etched after over 6.5 years of testing. Our conclusion is that at room temperature we are below the activation energy required to cause dissolution of polysilicon and hence we have not yet observed any dissolution related failures. This observation is in accordance with the acceleration model used in interpreting the high temperature tests. Indeed, it seems to confirm that the activation energy for the dissolution of the substrate or the top polysilicon is high. Accordingly, due to the exponential decrease of the acceleration factor with temperature, the dissolution of silicon or polysilicon may not be significant at the body temperature.

Out of the original 6 packages, one failed prematurely the first day and one failed because of mishandling. The 4 other devices are still under test and present no sign of leakage into the capsule after being soaked for 2216 days. Table 2 summarizes the data obtained from these soak tests.

Table 2: Data for room temperature soak tests in saline.

Number of packages in this study	6
Soaking solution	Saline
Failed within 24 hours (not included in MTTF)	1
Packages lost due to mishandling	1
Longest lasting packages in this study	2368 days
Packages still under tests with no measurable room temperature condensation inside	4
Average lifetime to date (MTTF) so far including losses due to mishandling	1919.8 days
Average lifetime to date (MTTF) so far excluding losses due to mishandling	2359 days

2.2 Wireless Monitoring of Humidity Inside Glass-Silicon Packages

A wireless humidity monitoring system (HMS) has several benefits. First, it greatly facilitates the in-vitro testing of the packages, decreasing the detection threshold of moisture (as compared to dew point sensors used in the room temperature saline tests) and reducing mishandling and temperature cycling. In addition, it would allow one to automate the in-vitro

testing procedure. Another benefit is that it allows continuous monitoring of humidity in packages that are implanted in animal hosts, thus providing important in-vivo hermeticity data.

In the previous quarterly reports, the wireless humidity monitoring approach is explained, which can be summarized as the following: a capacitive polyimide humidity sensor (HS) is wire bonded to an inductor made by copper wires wound around a ferrite core. This coil with the HS forms a LC tank circuit. The capacitive humidity sensor in this tank circuit responds to changes in humidity by changing its capacitance and thus the resonance frequency of the tank circuit shifts. When a coil (external antenna) is placed nearby this tank circuit; the maximum loading in the impedance measurements of the antenna is observed at the resonance frequency of the tank circuit allowing one to remotely monitor changes in humidity levels. We thus call the HS and the inductor combination the Humidity Monitoring System (HMS). Since the development of the fully integrated version of this device, the HMS is also referred to as the Hybrid Humidity Sensor (HHS).

2.2.1 High Temperature Soak Tests in Saline

An anodically sealed Humidity Monitoring System (HMS) has been soaking since April 1999 in phosphate buffered saline solution at high temperature. The package is inspected routinely under a microscope to detect any leakage path(s) on the phosphorous doped polysilicon bonding surface, and the resonant frequency of the HMS is measured to correlate this response with the humidity inside the sealed package. This data may provide useful information as to the failure and degradation processes of the package hermeticity. As of August 2001, neither a complete leakage path nor a corresponding HMS resonant frequency shift has been observed. Another indication that the package has not been compromised, is that the aluminum and copper metals of the humidity sensor and HMS coil are not corroded. Figure 4 shows the percent relative humidity change versus the number of days soaking at 97°C.

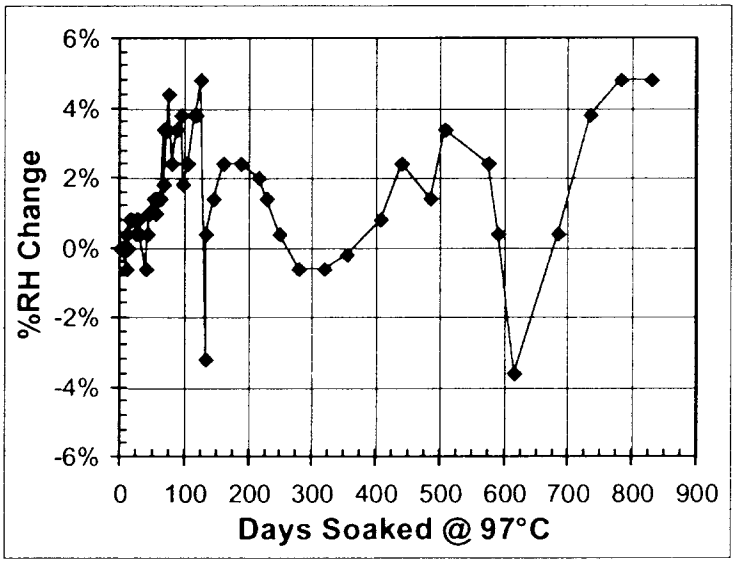

Figure 4: Telemetry data from a package soaked in high temperature saline soak test (97°C).

The frequency variations are attributed to day to day temperature fluctuations during testing. These variations are within experimental error and hence the HHS data and visual inspection analysis strongly suggest the anodically sealed package is hermetic for over 2 years 4 months.

2.2.2 In-Vivo Testing

With the development of the wireless humidity monitoring system, it is possible to remotely monitor package integrity while the device is implanted in an animal host. Consequently, six devices were prepared and screened to ensure hermetic seals. Each device passed a one-day room temperature soak in DI water to validate the seal prior to implant. The devices were then sent to the University of Michigan Medical School for implantation into guinea pig hosts. Two guinea pigs have been implanted with packages to monitor hermeticity in the in-vivo environment. Sites on the guinea pigs were selected to give the widest possible range of environmental conditions. On each host, one package was implanted into the leg, another into the abdomen, and a final one into the head for a total of three packages per host. Devices were implanted in the head beneath the skull but above the dura, under the skin but on top of the leg muscles, and in the abdominal cavity as depicted in Figure 5.

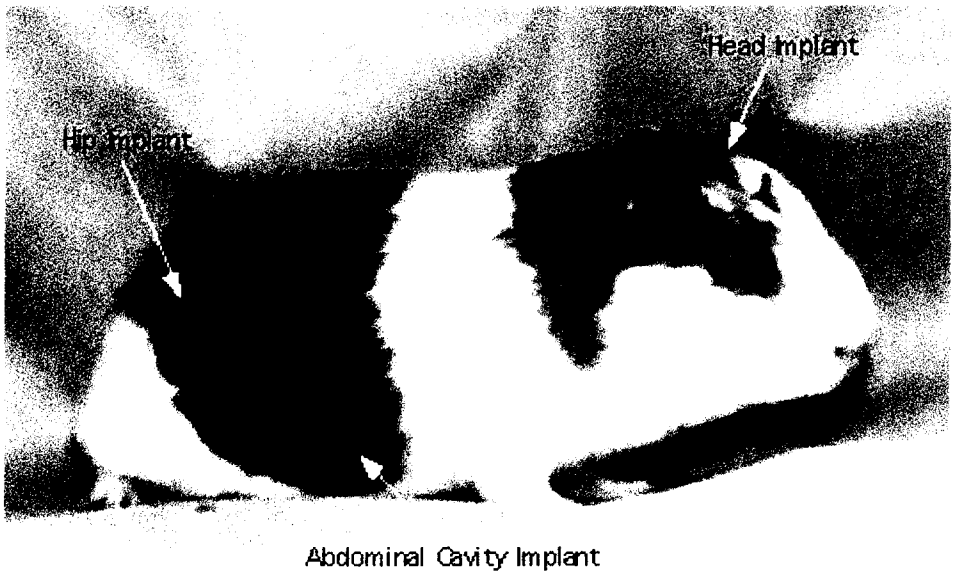

Figure 5: Locations of implanted packages in guinea pig host.

Tests were conducted immediately prior to and following implant, with no discernible change in system output. After this, devices were measured biweekly to detect shifts in resonant frequency resulting from changes of humidity in the package if any. Over the lifetime of these two animals there was no discernible shift in the output of any humidity sensing systems inside the packages. Given that a 50 kHz shift is considered significant, the output of the sensors, which varies by only a few kilohertz, indicates fairly steady humidity inside the packages. Figures 6 and 7 show the measured frequencies of the sensors over the duration of the test.

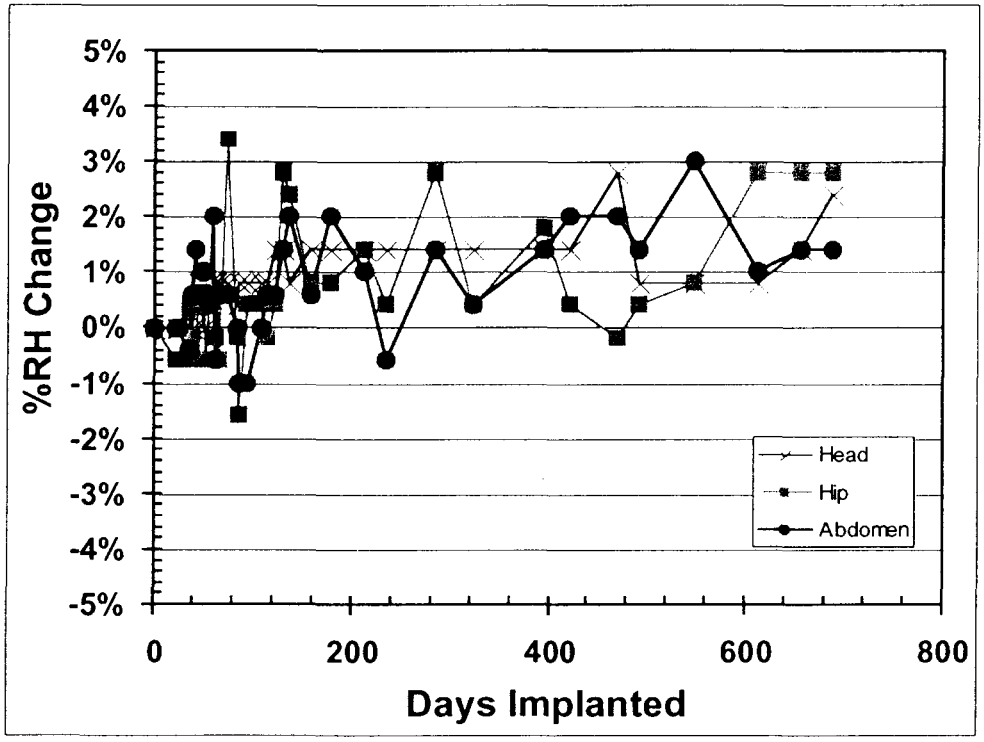

Figure 6: %RH change measurements over time for Guinea Pig A.

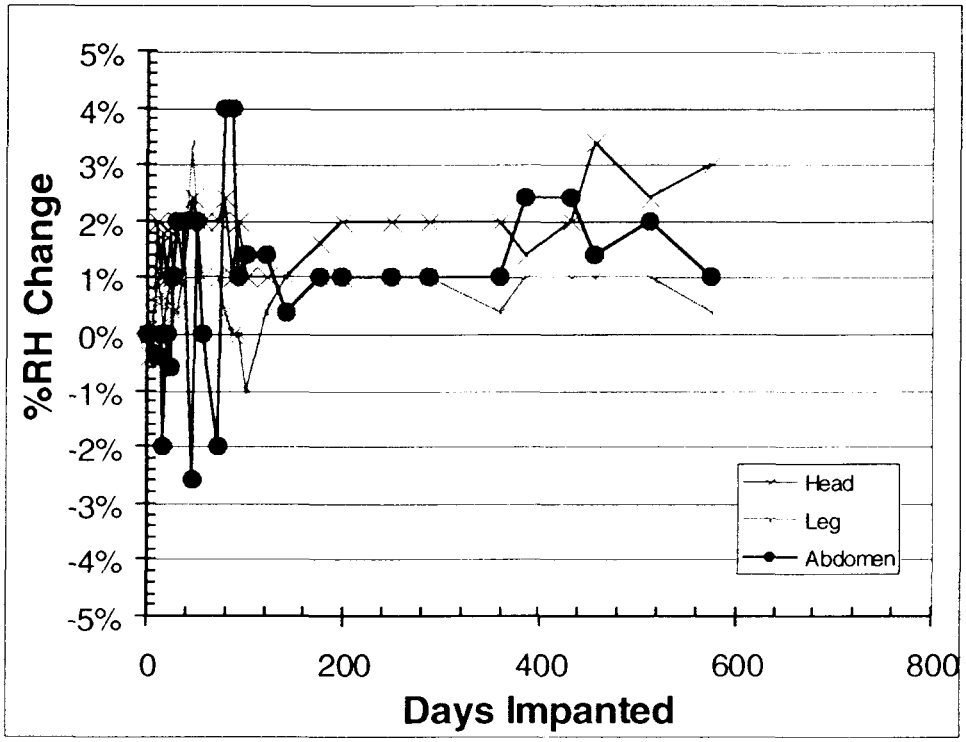

Figure 7: %RH change measurements over time for Guinea Pig B.

Guinea pig B died due to unknown causes on January 23, 2001. Unfortunately, a histology examination could not be conducted on this animal since the animal tissue was not perfused. Another guinea pig was implanted with three packages (guinea pig D) for a one-month period. Guinea pigs A and D were sacrificed and the packages explanted. Gross inspection of the explanted packages from guinea pigs A, B, and D have been conducted. No visible etch progressions nor damage to the package was visible. Table 3 summarizes the humidity monitoring results from the packages implanted in guinea pigs A and B.

Table 3: Data from packages implanted in guinea pigs A and B.

Number of packages in this study	6
Maximum number of days in guinea pig A	688
Maximum number of days in guinea pig B	574

The hybrid humidity sensors were removed from the packages however the HHS implanted in the head and leg were damaged while attempting to break the glass capsule from the silicon. Figure 8 shows the response of the HHS implanted in the abdomen of Guinea Pig B.

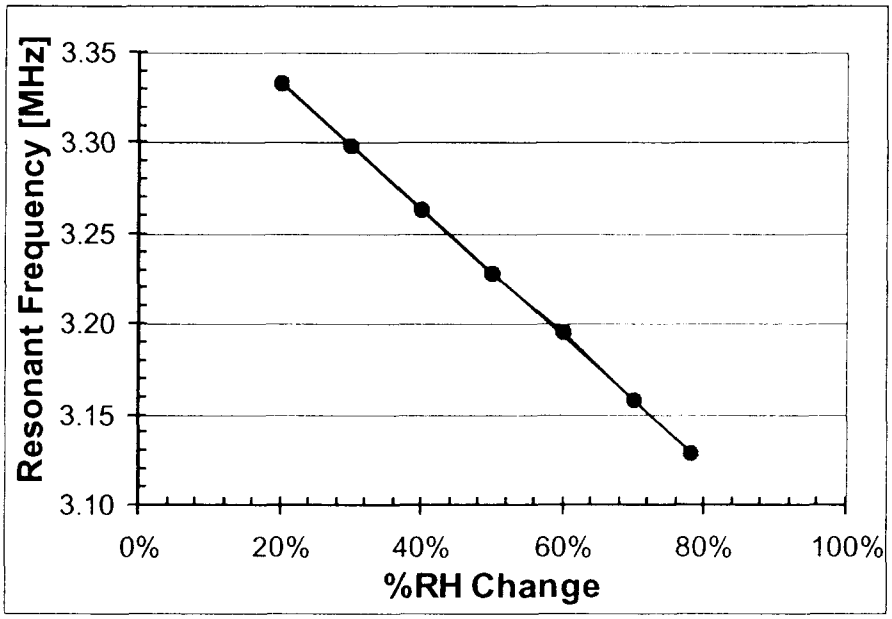

Figure 8: HHS response to humidity after removal from Guinea Pig B.

The observed resonant frequency change in response to changes in humidity of the HHS along with the data from the same sensor shown in Figure 8, confirms that the package remained hermetically sealed while implanted in the guinea pig.

The University of Michigan Medical School is currently preparing and studying the tissues and bone that surrounded the packages.

2.3 A Passive Wireless Integrated Humidity Sensor

A single-chip integrated wireless humidity sensor (IHS) has been developed to address the deficiencies of the hybrid wireless humidity sensor discussed in the September 1999 NIH report and summarized in Table 4.

Table 4: Deficiencies of the hybrid HMS design

– Tedious time consuming fabrication
– Multiple component system – low yield
– Variation of performance due to hand assembly
– Large device size

A drawing of the integrated humidity sensor is shown in Figure 9. The equivalent circuit of this design, shown in Figure 10, is an LC tank circuit where the inductor, with inductance L and series resistance R, is the planar copper coil and the capacitor, with capacitance C, is between the copper coil and the conductive silicon substrate separated by humidity sensitive polyimide as shown in Figure 11. Note that the circuit model is exactly the same as the hybrid humidity sensor model.

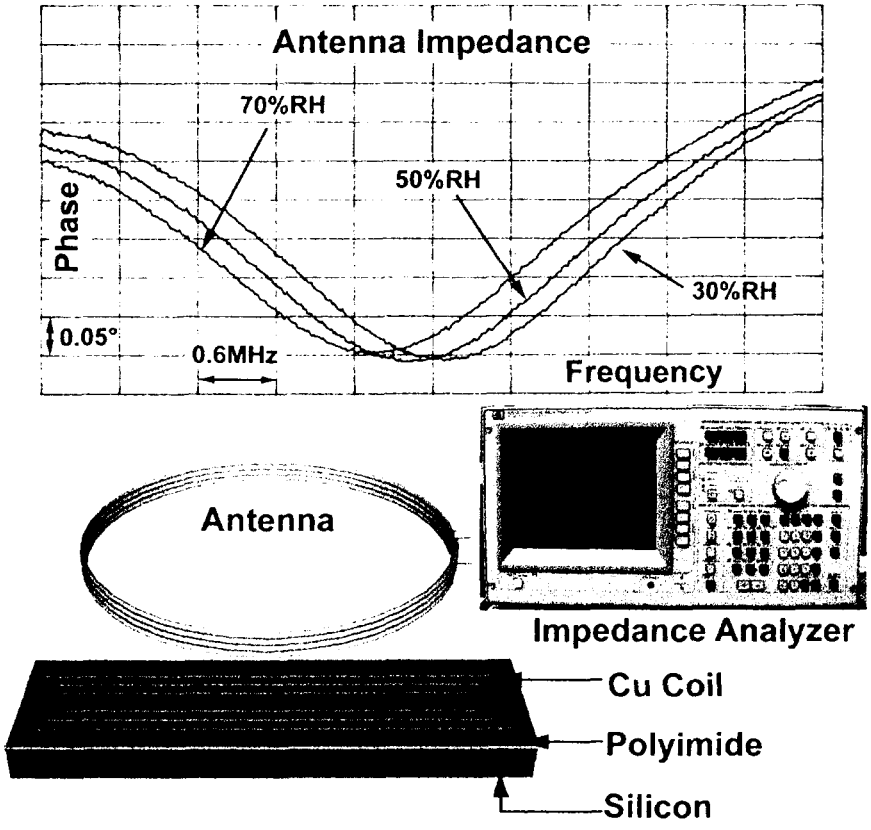

Figure 9: A passive wireless integrated humidity sensor design.

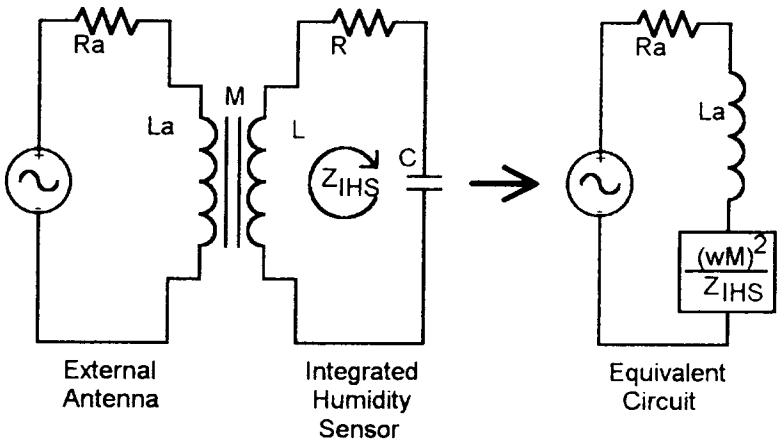

Figure 10: IHS equivalent circuit model.

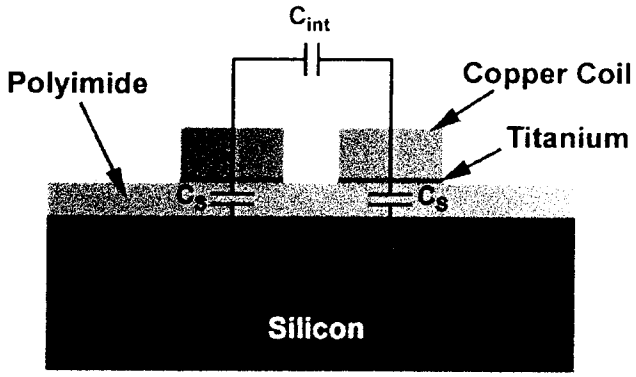

Figure 11: Circuit elements of the HIS.

An SEM photograph of the IHS is shown in Figure 12. A typical impedance measurement is shown in Figure 13.

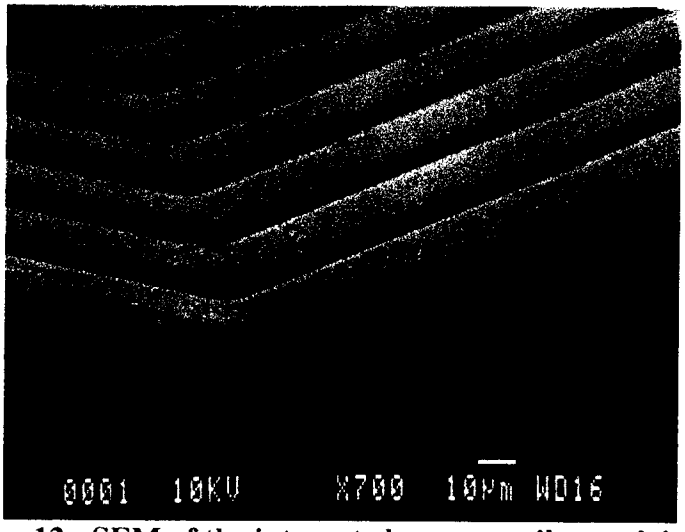

Figure 12: SEM of the integrated cupper coil on polyimide.

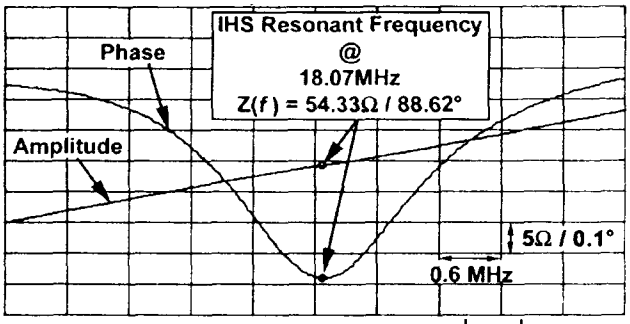

Figure 13: Impedance measurements $|Z(f)|$ and $\angle Z(f)$.

A paper entitled "A Passive Wireless Integrated Humidity Sensor" was accepted for publication in a special edition of Sensors and Actuators Journal.

2.4 Packaging experiments for the neural Probes

As part of our work on hermetic biocompatible packaging, we would like to extend our technology to devices other than the microstimulator. One obvious potential application of this technology lies in the development of a packaging technology for active neural probes. The active neural probe is designed to record neural signals at multiple sites, but has been heretofore limited to acute implants because there was no adequate package to protect the circuitry for long term implants. As a result, we are adapting our packaging technology to develop a hermetically sealed neural probe for chronic implantation. The most recent research into neural probes has focused upon using electroplated films to seal the probe. A relatively thick film of gold should provide a long-term hermetic seal for the probes. Figure 14 shows the concept of the packaged neural probe.

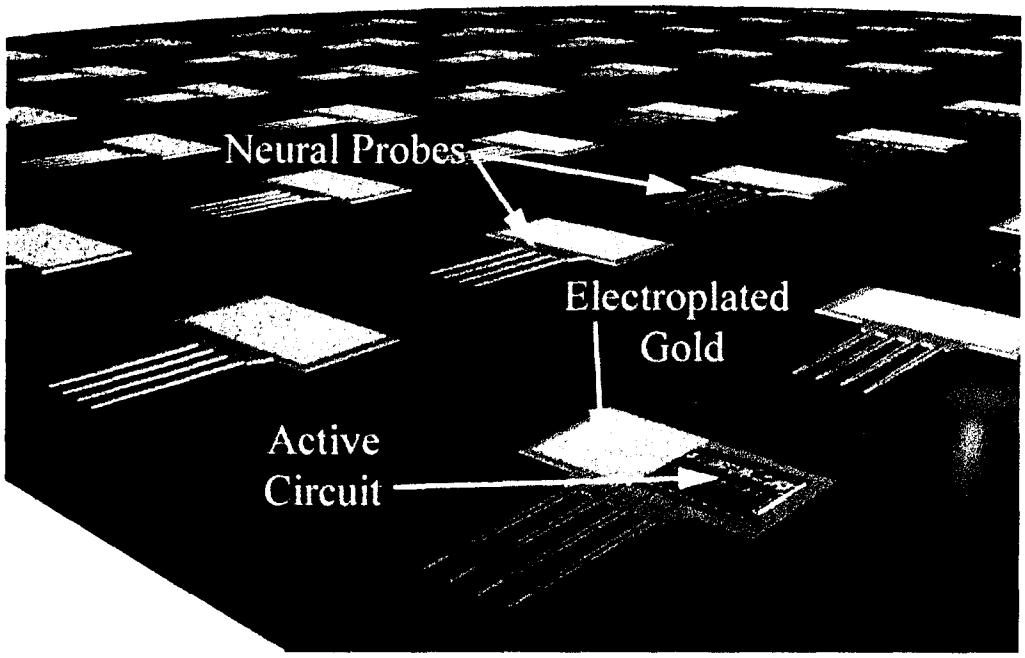

Figure 14: Schematic of packaged Neural Probe.

In the past quarters, we have demonstrated that probes made with this technique are capable of demonstrating acute hermeticity. However, long-term test data was still needed to predict the MTTF of these structures

In order to generate long term measurement data, a test structure has been designed that will accurately measure package lifetime. This test structure is depicted in Figure 15.

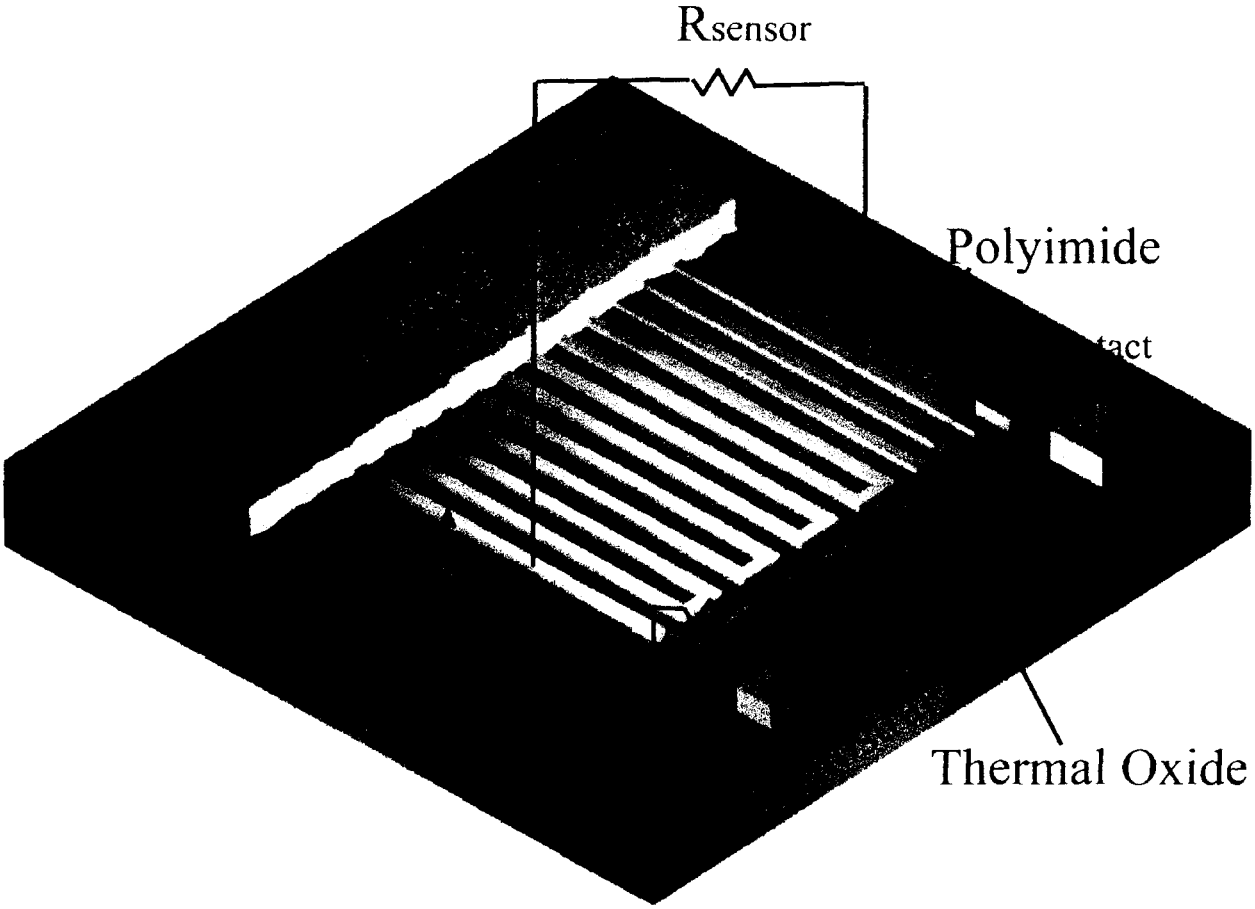

Figure 15: Test structure for long-term low profile soak tests.

This test structure utilizes an aluminum resistor that runs the length of the package. The resistor will corrode in the presence of saline, thus changing resistance. The integrated saline sensor was characterized by placing it in a solution of PBS at 95°C and measuring the resistance across the terminals. To perform this test, a fully packaged sensor was cut with a razor blade, removing the gold and polyimide, while keeping the resistor intact. The sensor was then glued to a metal hybrid package and a LABVIEW program was written to monitor resistance at 20-second intervals. The saline was preheated for 3 hours to raise the temperature to 95 C and the program was then started. After 360 seconds, the sensor was placed in the solution. Figure 16 shows the dynamic response of the sensor to saline. After 40 seconds, there is a marked rise in resistance from 720W to 11kW. This is close to the contact resistance of the solution, which is substantially lower than the open circuit resistance. When the sensor is removed from the solution, resistance is measured at an open circuit value of 10^{37}W.

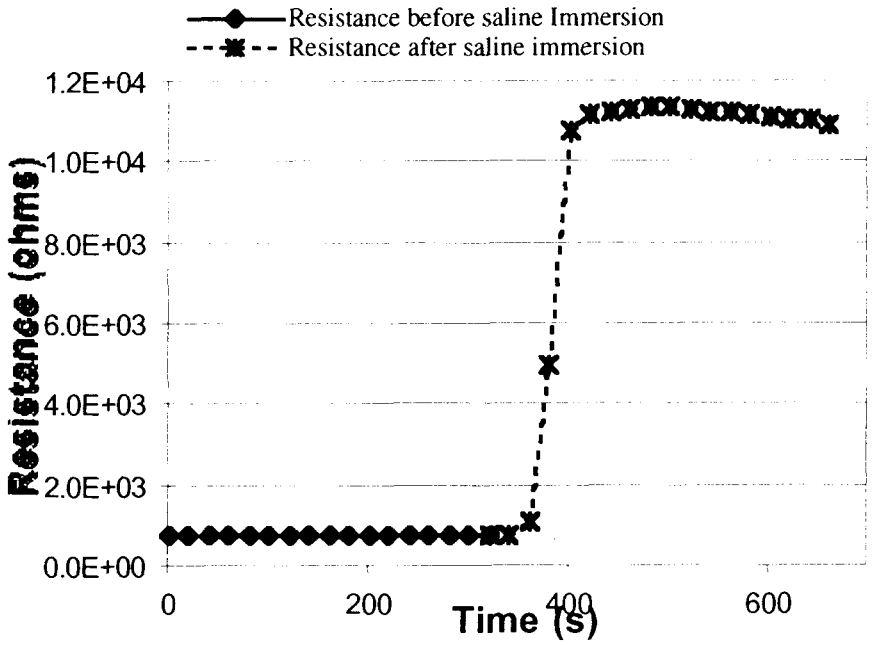

Figure 16: Dynamic response of the integrated saline sensor immersed in PBS at 95°C.

To test this structure, an automated test station was constructed. Shown in Figure 17, this station utilizes a multimeter connected to an array of resistors through a GPIB bus and a DAQ card. This station enables us to evaluate the chronic stability of this package.

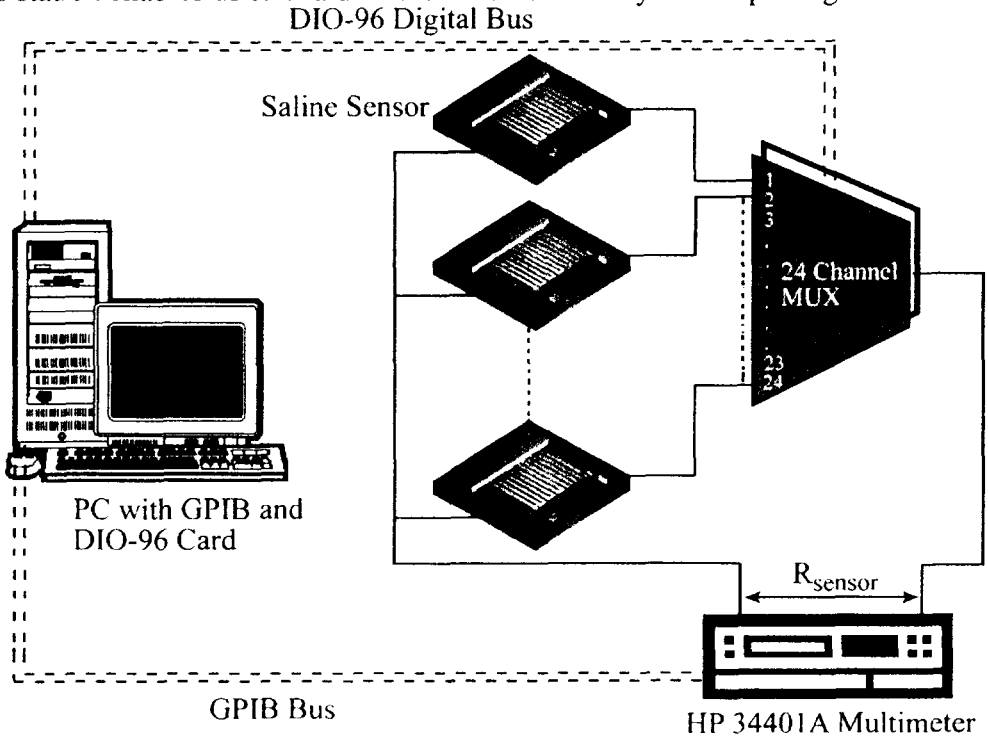

Figure 17: Automated test station for chronic monitoring of package.

Twenty-four packaged sensors were fabricated. The sensors were glued and wire bonded to a metal hybrid plug-in package with twelve devices placed on each package. One hybrid package was then soaked in phosphate buffered saline (PBS) in an oven set to 85°C while the other package was placed in PBS at 95°C. The hybrid packages were removed daily and tested via an automated testing station running on a PC. This test continued until the last sensor failed. A picture of the metal hybrid package with the 12 sensors packaged on it is shown in Figure 18.

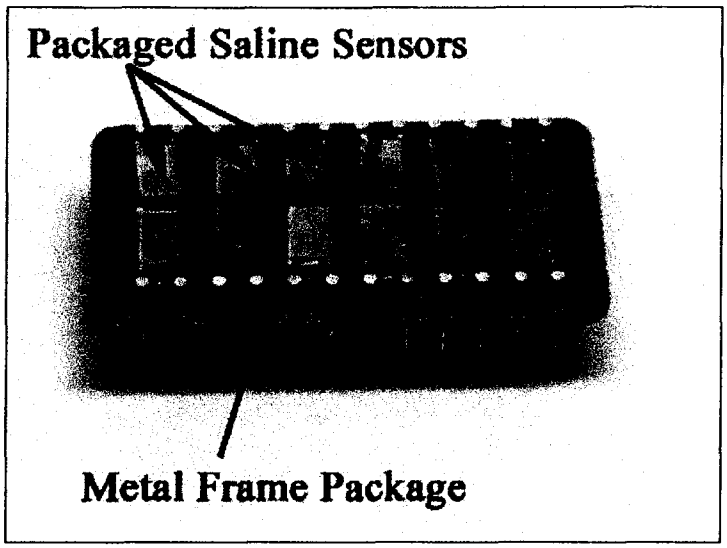

Figure 18: Metal Frame Package with packaged saline sensors.

The automated test of 24 packages lasted for two months, with the results summarized in Table 5. There was a high incidence of infant mortality in the sample set at 95°C while failure did not occur in the 85°C sample set until 20 days into the test. A failure was defined as a resistance change of 2 orders of magnitude. Failures were usually accompanied by a noticeable bubbling of the gold film. The proposed mechanism for failure is outgassing of trapped moisture in the polyimide. The moisture likely cracks the gold film, allowing saline to reach the polyimide and eventually attack the sensor. This moisture is introduced during processing. The electroplating mold photoresist is developed in wet chemicals and rinsed for three minutes in water. During this time, water seeps into the polyimide through pinholes in the sputtered film and is trapped in it. The moisture then will outgas during the high temperature soak test.

Table 5: Results of the automated lifetime test.

Temperature	85°C	95°C
Number of packages in study	12	12
Packages failed within 24 hours	0	4
MTTF	30.54 days	7.98 days
Longest lasting package	57.96 days	24.96 days

Using this data it is possible to extract a lifetime. If it is assumed that an Arrhenius relationship exists, with failures occurring in a process that is exponential with temperature, then one can extract the MTTF at the body temperature of 37.5°C. In this model, the MTTF can be expressed as:

$$MTTF(T) = R_0 \exp\left(-\frac{E_a}{K_b T}\right)$$

In this equation, the two fitting parameters are, R_0, the pre-exponential factor and the activation energy, E_a. With two data points, it is possible to fit a line through the data, although there will be no corroboration of the curve fit. Using this technique, the activation energy is measured as 1.52eV and R_0 is measured to be 1.1×10^{-20} days. This gives a MTTF at 37.5°C of 160 years. However this data is still preliminary and there are several issues to be addressed. Due to the exponential nature of the Arrhenius Relationship, slight variation in temperature can have a drastic impact upon MTTF predictions. The ovens used in these tests have a temperature stability of only ±4°C, which generates concern over the accuracy of this data. The results of this testing were presented in a paper entitled "An Ultra-Thin Hermetic Package Utilizing Electroplated Gold" at the Transducers 2001 Conference in Munich.

In order to overcome the experimental problems encountered with the first set of tests and to improve the overall reliability of the data, new test structures and a new experimental setup was devised. To improve the overall temperature stability, 3 dry bath incubators, which have temperature resolution and control of 0.1°C, were ordered. Custom heating blocks were constructed to encase the glass capsules that hold the packaged saline sensors. This setup was calibrated for temperature profile for 3 different temperatures, with Table 6 showing the desired temperature and the measured temperature within the 2 glass jars in each of the 3 dry baths.

Table 6: Measured temperatures in the 6 sample sets.

Set Temp	85 °C	90 °C	95 °C
Jar A	84.7	89.8	94.7
Jar B	85.3	90.2	95.1

This new setup represents an order of magnitude improvement in temperature control and should lead to more confidence in our test data. Figure 19 shows the improved temperature control test setup with soaking samples.

To improve the package technology, we attempted to isolate failures in the gold package from failures in the polyimide. To do this, we fabricated saline sensors with sputtered SiO_2 as a dielectric spacer instead of polyimide. The structures had a similar dynamic response to saline and 72 devices were fabricated and packaged on metal hybrid packages. These devices were then soaked in saline at elevated temperature. While these tests are still in progress, the data should be available in the next quarter.

This packaging technology has also been transferred to the neural recording project at Michigan. Active probe designs with integrated saline sensors packaged under electroplated gold have been made. These probes will be fabricated in the coming quarter and when finished,

will allow us to generate in vivo chronic recording and package stability data. A further improvement allowed by this technology is that the package should substantially decrease the optical sensitivity of previous probe designs.

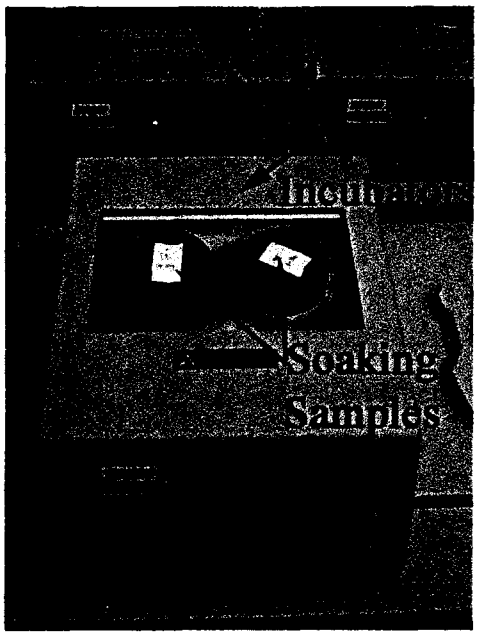

Figure 19: New Dry Bath Incubators for improved temperature control.

3. Improved Design of the FINESS Chip

In previous progress reports we had presented the design and operation and demonstrated the feasibility of the idea for a single-chip fully-integrated nerve-stimulating system (FINESS). Although the basic circuit blocks in this initial design worked and demonstrated basic operation, these circuit blocks needed to be redesigned and optimized so they could function properly under changing conditions. During the past quarter efforts were undertaken to redesign and optimize some of the circuit blocks in FINESS as reported below. Note that only the redesigned circuit blocks are discussed in this report. All building blocks are simulated with device model parameters of the in-house 3μm BiCMOS process.

3.1 Front-End Blocks:

The front-end part of the FINESS chip consists of the coil, power regulator, clock recovery, envelope detector, and power-on reset. In FINESS1 (i.e., the original FINESS chip) experiments:

- Power-on reset block showed unconditional perfect operation;
- Clock recovery and envelope detector blocks were working in a limited supply range; and
- In power regulation block:
    - The full-wave rectifier had leakage problems caused by the nature of the BiCMOS process used;

- The voltage regulator operated over a narrow frequency range and was sensitive to large input amplitude variations associated with ASK modulation.

3.1.1: Power Regulator:

This section deals with the redesign of the voltage regulator. Open-loop configuration is considered for the required voltage regulator since the original design was an open-loop regulator with a simple Zener reference. Since the problem had been observed only in its reference voltage, its reference voltage generator is replaced with an improved circuit. It should be added that because of its simplicity, this configuration seems more suitable for the U of M 3.0μm BiCMOS process.

Supply-Independent Voltage Reference:

Because of the relatively poor performance of the Zener diodes in the in-house BiCMOS process, the voltage reference in FINESS1 was not working as desired in the presence of large ripples on the input unregulated voltage, especially at high frequencies.

Figure 20(a) shows the schematic diagram of the well-known V_{GS}-referenced supply-independent current reference circuit, which has been so optimized that can be used as a CMOS supply-independent voltage reference circuit as well. This optimization, which lets the circuit to utilize a self-compensating mechanism, allows the circuit to produce a constant and robust reference voltage along a wide range of input unregulated voltage. DC transfer characteristic for the above supply-independent voltage reference, optimized for Vdd(max)=20V, is shown in Fig. 20(b).

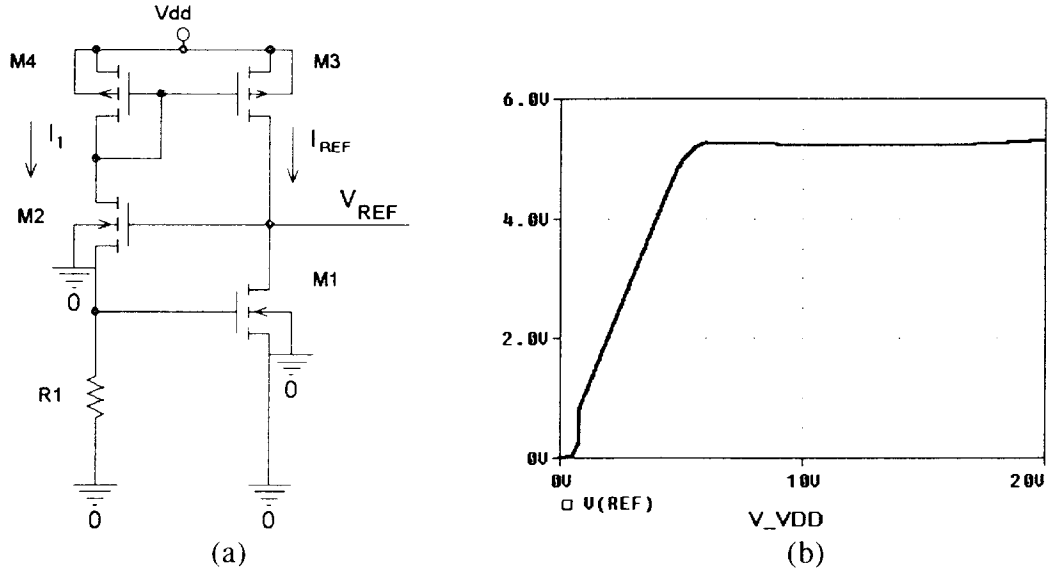

Figure 20: Proposed CMOS voltage reference (a) Circuit schematic; (b) DC transfer characteristic.

Dynamic Behavior:

Although the DC characteristic curve for the voltage reference circuit is quite flat for Vdd greater than Vdd(min), it only shows static dependency of the reference voltage on Vdd variations. However, voltage ripples on the unregulated supply rail (Vdd), appear as a dynamic component and affect the reference voltage with a completely different mechanism. Figure 21(a) illustrates the Bode magnitude diagram, which shows the transfer gain from the unregulated supply voltage to the output reference voltage. As can be seen the transfer gain is –43.3dB that is very good, but it is degraded for above 1MHz. As we know, in our application ripples on the unregulated voltage are at 8MHz ($=2f_{RF}$) and 25kHz (f_{data}). Frequency characteristic curve of Figure 21(a) shows that the circuit can't reject high-frequency ripples as well as low-frequency ones. In order to compensate the effect of the "zero" at 1MHz in the Bode diagram of Figure 21 (a), a stabilizing capacitor is placed between the reference node and ground in the schematic diagram of Figure 1(a) which cancels that "zero" by adding a "pole" at the same frequency. Figure 21(b) shows the effect of adding a stabilizing capacitor with different capacitance values on the frequency response of the voltage reference circuit.

Start-up Circuit:

The proposed reference voltage generator, like many other similar supply-independent current/voltage reference circuits, has two stable operating points: one at zero current, and the other at the desired point of operation. Such circuits, as we know, require start-up auxiliary circuits in order to prevent them from operating in the undesired state. As is shown in Figure 22, a simple differential amplifier is used as the start-up circuit. Based on the current steering idea when the reference circuit is at zero-current state and hence the reference voltage is near zero, the start-up circuit starts sourcing current through Msu2 and Dsu4 into M1, which causes the circuit to leave the zero-current state. As the reference circuit arrives its desired operating point, the start-up current changes its way and goes through Msu1 and Dsu1~Dsu3, rather than Msu2 and Dsu4.

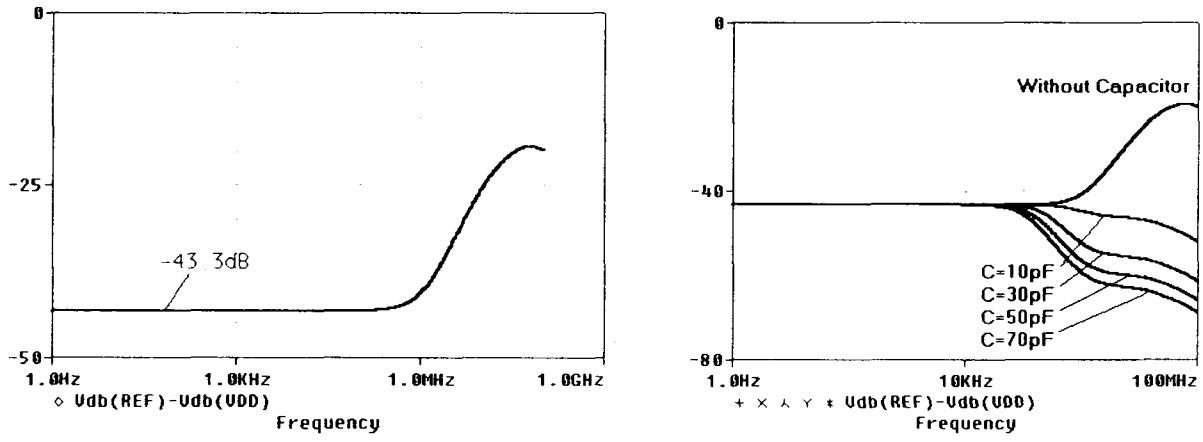

Figure 21:Ripple rejection characteristic in frequency domain characteristic (a) for the CMOS voltage reference of Fig. 20(a), (b) after adding the stabilizing capacitor.

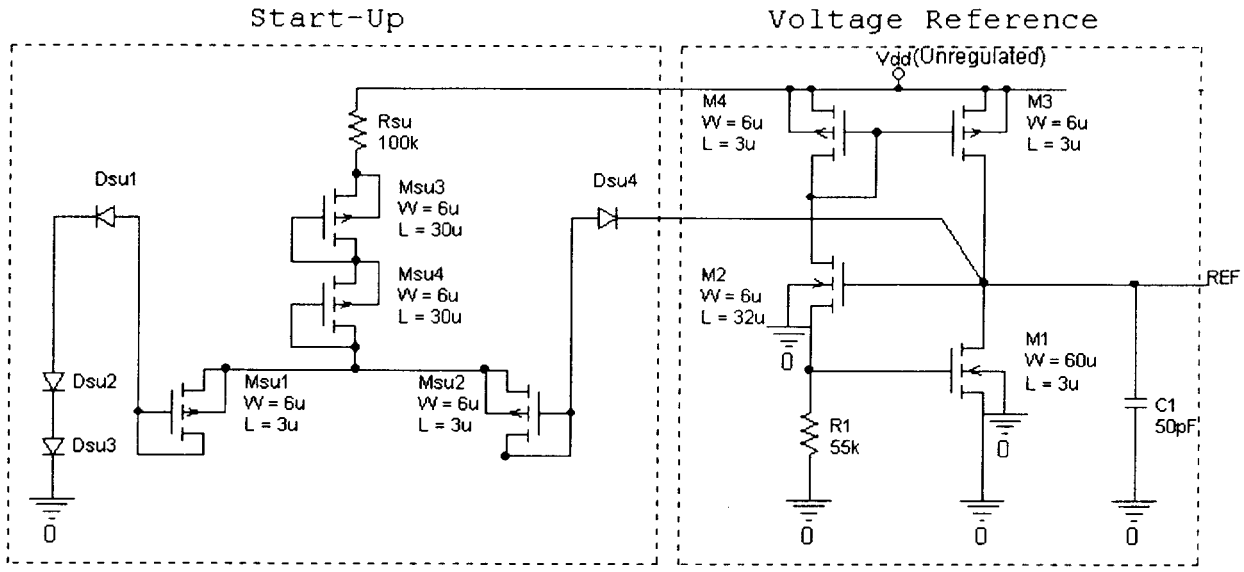

Figure 22: Adding the startup circuit to the CMOS voltage reference.

Voltage Regulator:

The simplest way to design a voltage regulator by using the above-mentioned voltage-reference circuit is to buffer it by a Darlington pair. The schematic diagram of the optimized open-loop voltage regulator, including the start-up circuit, is shown in Figure 23.

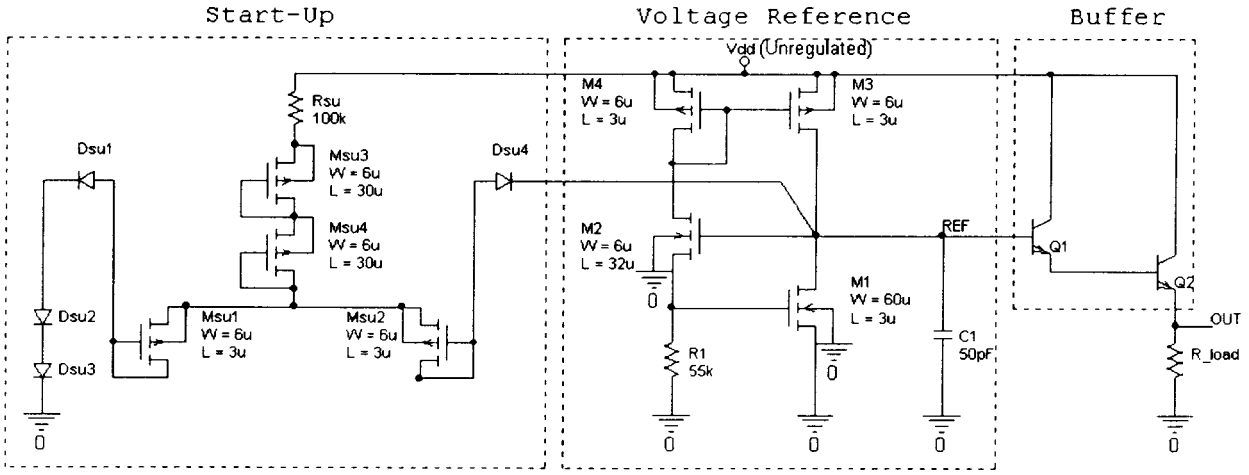

Figure 23: Complete voltage regulator block.

Figure 24 shows the load regulation characteristic for the regulator of Figure 23 along with its reference voltage. Also, in the case of minimum possible value for the unregulated input voltage, load current (I_load) and current consumption of the start-up circuit and the reference voltage generator (I_regulator) are shown in Figure 25. I_regulator is only 30~40μA for the case

shown in Figure 25, and increases to 110μA when the unregulated supply voltage is as high as 20V.

In order to supply the circuit by a real input voltage, a 4-MHz RF carrier is ASK-modulated by a 25kHz data (80% modulation index), full-wave rectified, and low-pass filtered, and is then considered as its input. However the circuit of Figure 22 works with input RF peak amplitudes as low as 7V/8.75V (for LOW/HIGH data), adding buffer transistors and a 1kW resistive load leads to much more current sinking from the storage capacitor after the rectifier and consequently larger ripples across it. It is clear that in order to keep the above minimum acceptable input amplitude, the storage capacitance should be increased. In this design, it is decided to maintain the same storage capacitance that was used in FINESS1. So, the minimum acceptable input ASK-modulated RF peak amplitude increases to 10V/12.5V (for LOW/HIGH data) again for a 1kW load.

Figure 26 shows the unregulated supply voltage, reference voltage, and the output voltage in the final voltage regulator of Figure 23 for an input ASK-modulated RF peak amplitude of 10V/12.5V (for LOW/HIGH data) and a 1k resistive load.

Simulation results for the designed voltage regulator are summarized in Table 7.

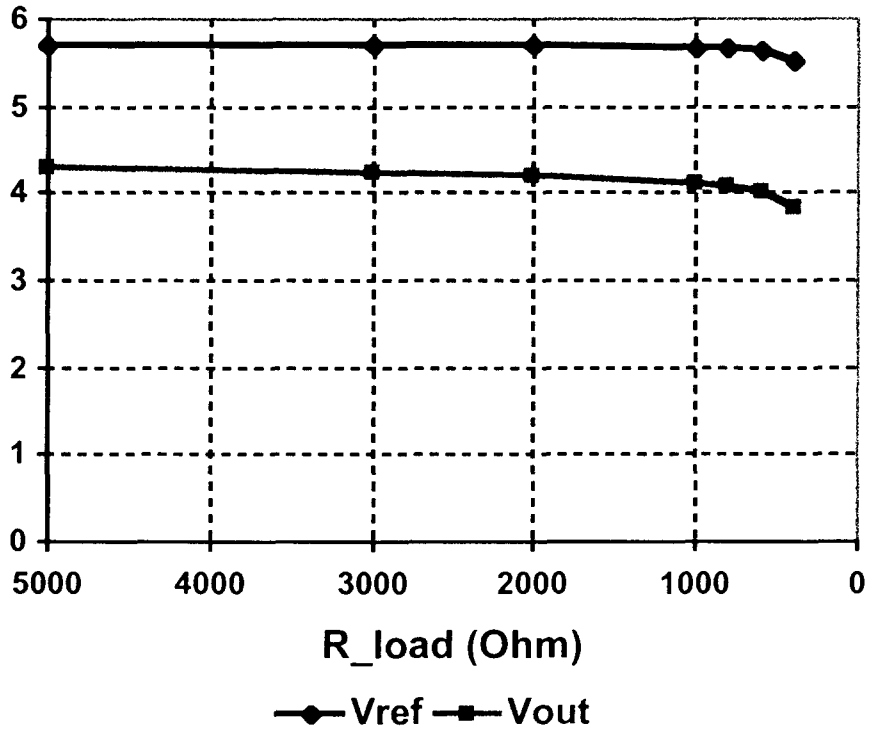

Figure 24: Load regulation characteristic for the regulator of Figure 23.

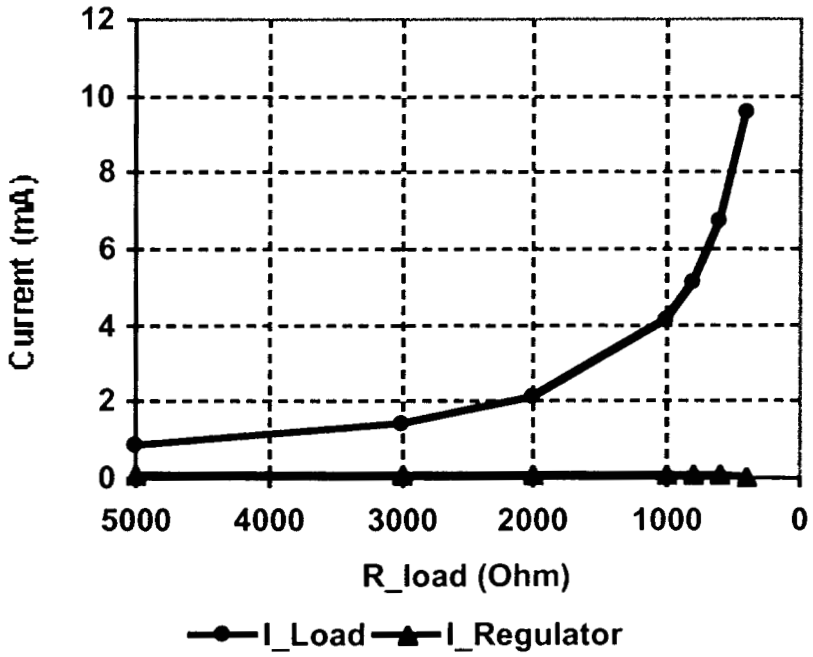

Figure 25: Load current (I_load) and current consumption of the start-up circuit and the reference voltage generator (I_regulatorfor the minimum unregulated input voltage.

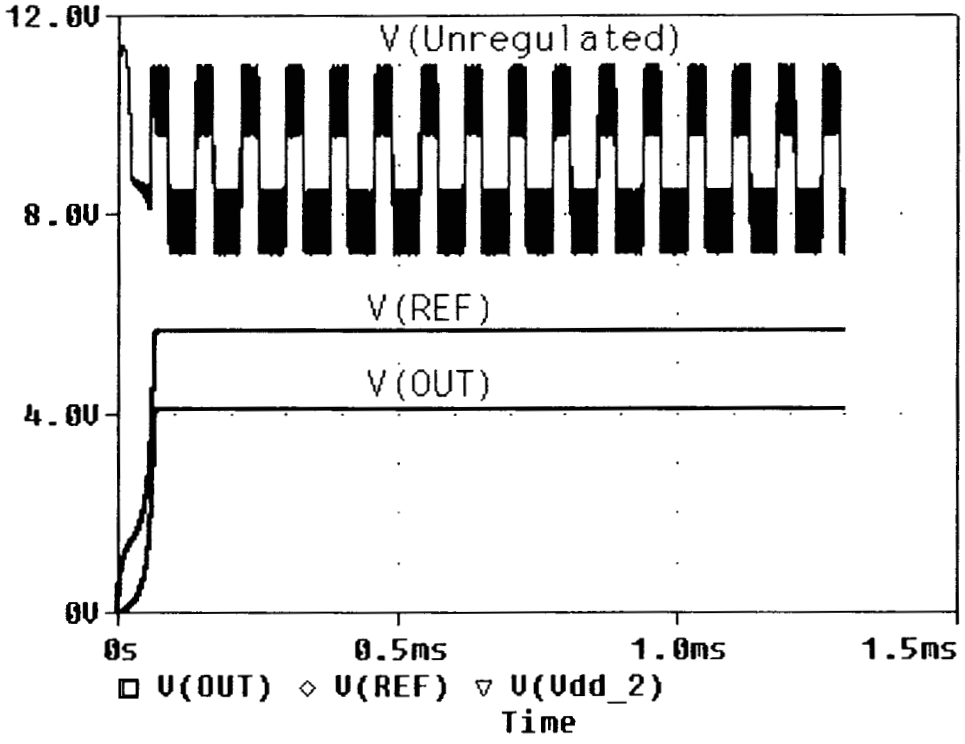

Figure 26: Unregulated supply voltage, reference voltage, and the output voltage in the final voltage regulator of Figure 23.

Table 7: Simulation results summary for the designed voltage regulator

Specification	Value
Output voltage	4.1V @ 1kOhm load
Min. required peak amplitude for the received voltage*	12.5V for HIGH/10V for LOW
Ripple content at the output	29mV, 1kOhm load
Pure regulator current consumption (excluding load current)	40uA@ min. input peak amplitude, for 1kOhm load

*Based on the initial FINESS chip design, the transmitted RF voltage is supposed to be an ASK-modulated signal with carrier frequency of 4MHz, data rate of 25kHz, and modulation index of 80%.

In order to consider the possibility of trimming the circuit against process variations, resistor R1 in the regulator has been implemented as shown in Figure 27. R1, which is a poly resistor and is supposed to be 55kW, is realized by a 45kW resistor and a series combination of 10kW, 5kW, 3kW, 2kW, and 1kW resistors, each shorted by a metal link. This way, having fabricated R1 within –17% and +22% of its nominal values, the above-pointed combination of resistors and links will allow us to have a 55kW resistor. Also, transistor Ms2 is considered in series with M1 shorted by a link. This transistor can be used to decrease W/L ratio of M1 if necessary.

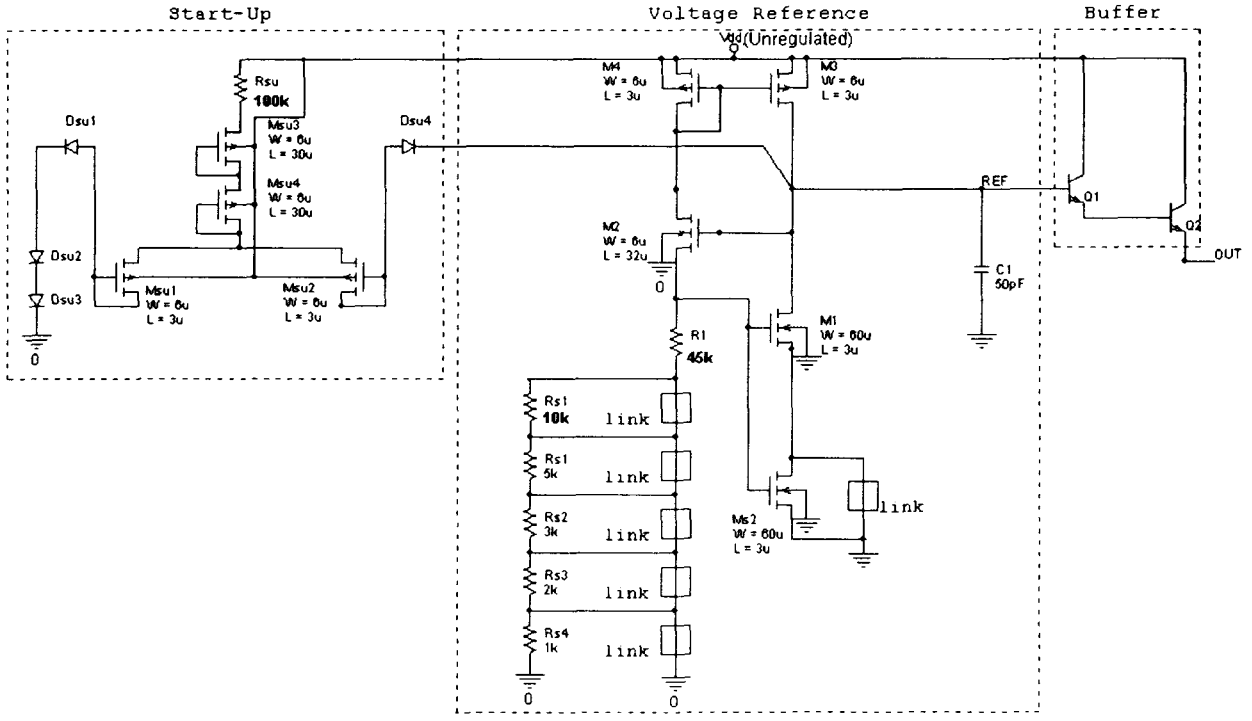

Figure 27: Circuit design to accommodate trimming using on-chip resistors after fabrication.

3.1.2: Clock Recovery

The clock recovery block has been improved so that it can operate at large amplitude switching edges associated with ASK modulation, whereas the previous version of the circuit failed to recover the clock. To achieve this, the feedback loop has been redesigned to obtain a self-oscillating behavior, when the above amplitude edges occur. This modification has been originally done by Mr. Maysam Govanloo as part of his circuit for use in multichannel stimulating probes.

Another improvement in the clock recovery block is the replacement of its bipolar transistor by an NMOS transistor, resulting in a full-CMOS circuit.

The final circuit is shown in Figure 28. It should be added that the resistor R_{bias} has been also implemented by some partial resistors some of them shorted by their associated links.

Although the circuit has been designed for ASK modulation index of 80%, it works well for modulation indexes down to 55% when the maximum amplitude of the input is 20V, and for modulation indexes down to 30% when the maximum amplitude of the input is 13V. Essentially the circuit works more easily with higher modulation indexes, and the above values determine the minimum modulation indexes required for proper operation. Figure 29 shows the input and output waveforms for the modified envelope detector circuit, when the input RF voltage with 16V amplitude is ASK-modulated with modulation index of 75%.

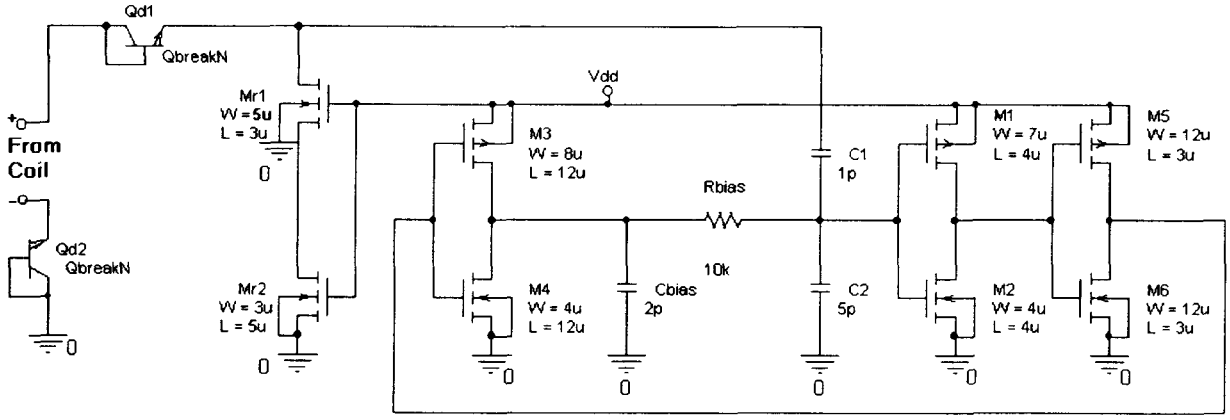

Figure 28: Circuit schematic for the clock recovery block.

3.1.3: Envelope Detector:

FINESS1 experimental results verified that the envelope detector circuit used in FINESS1 was working worse than the circuit used in Mark Nardin's circuit which was developed for a multichannel microstimulator previously reported. Hence, it was decided to use the circuit used in Nardin's thesis after some modifications by Mr. Maysam Govanloo. Re-simulating this envelope detector for the second version of FINESS shows that it works well in our operating conditions without needing any modification. However the circuit has been designed to work with 4V supply voltage, it also works with supply voltages down to 3.3V for

80% ASK modulation index. It should be noted that the maximum modulation index for the circuit is 80%, and it continues working more easily with lower modulation indexes.

Figure 30 shows the schematic diagram of the envelope detector block.

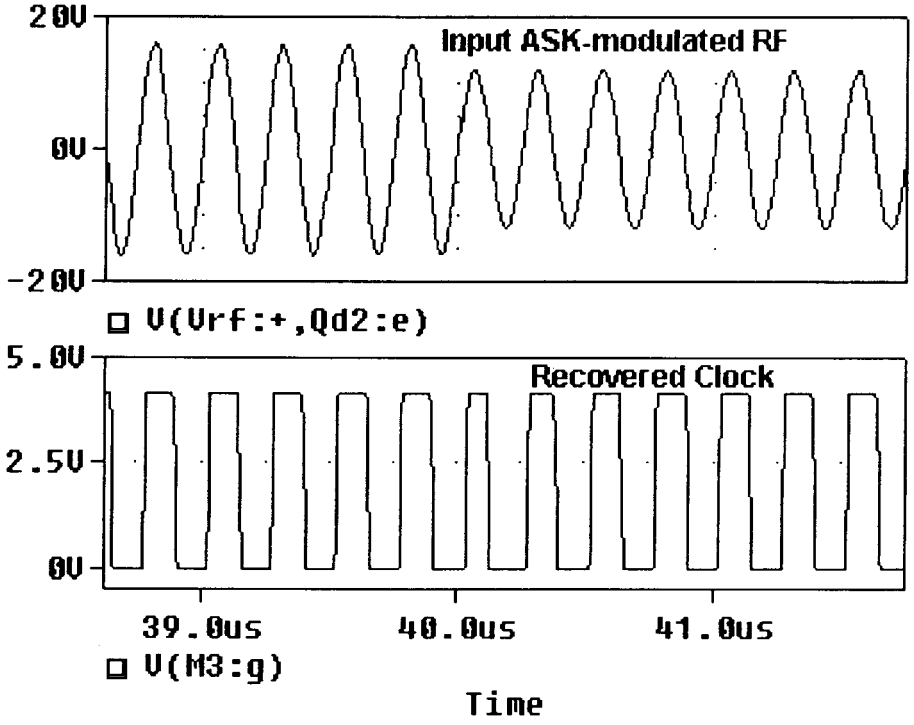

Figure 29: Input and the output waveforms for the clock recovery block.

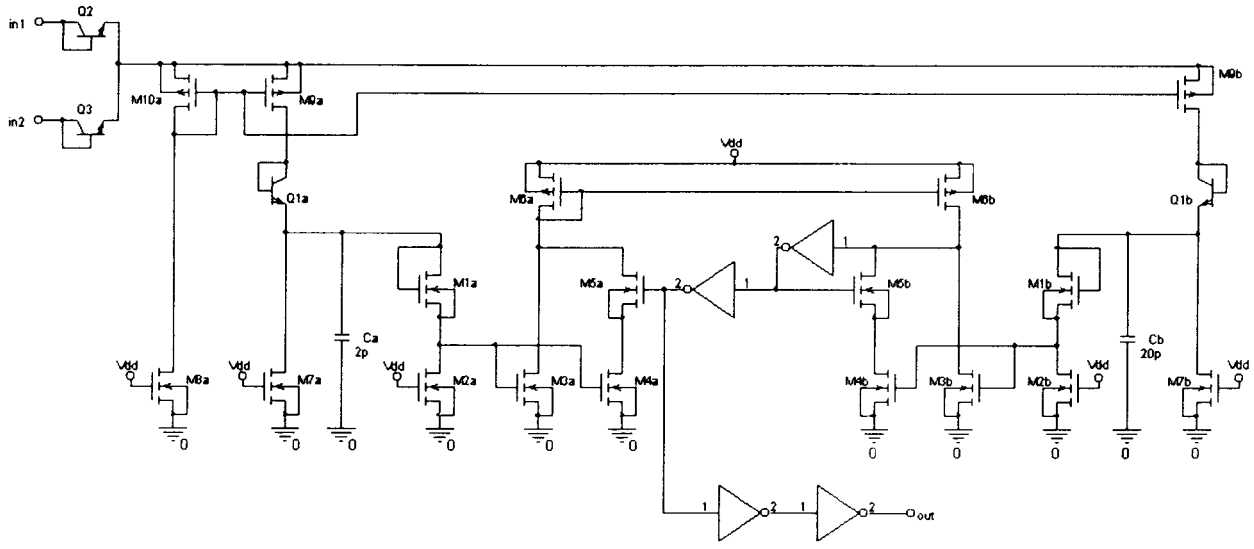

Figure 30: Circuit schematic for the envelope detector block.

3.2 Digital Circuitry:

In some conditions there was observed improper operations in a specific latch in FIINESS1. In order to fix the problem, it was necessary to change the transistor-level implementation of the latch. Also, some parts of the finite-state machine had been designed in pass-transistor logic style. These parts were also preferred to be redesigned with conventional static CMOS, which is a more reliable logic style.

Figure 31 shows the simplified block diagram for the second version of FINESS chip. thelayout of the whole system is shown in Figure 32, which occupies a 2.83mm×9.891mm area.

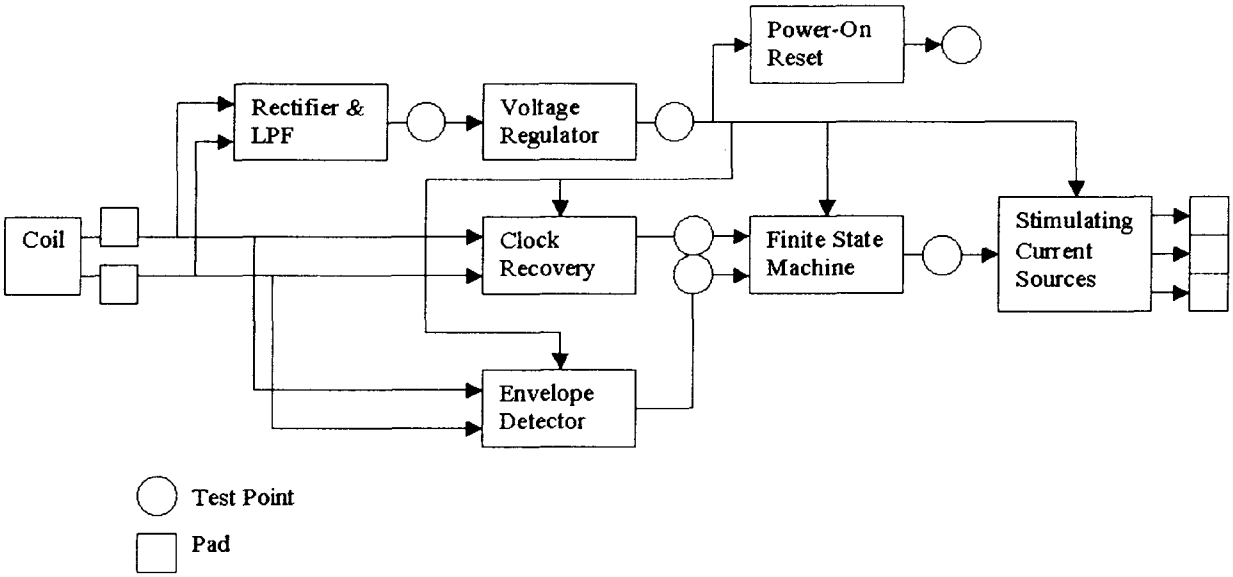

Figure 31: Simplified block diagram for the second version of FINESS chip.

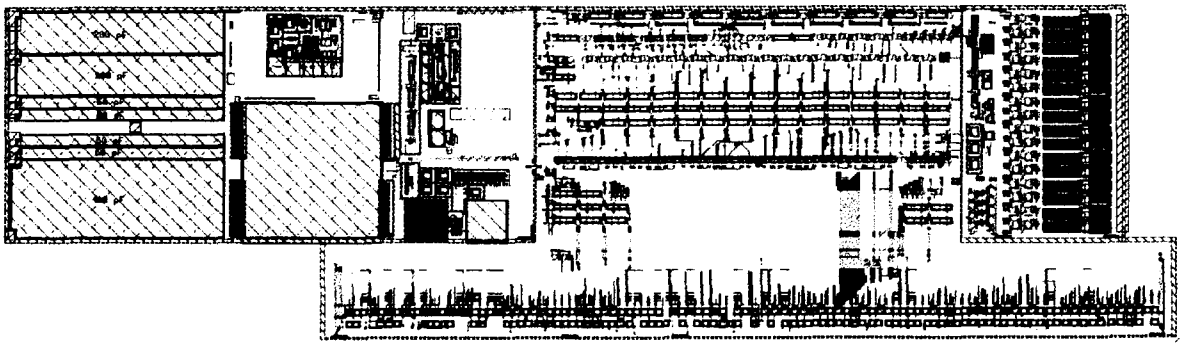

Figure 32: Layout of the second version of FINESS chip.

III. PLANS FOR THE COMING QUARTER

In the coming quarter we will complete histology tests on the tissue extracted from the guinea pigs implanted with packages, and will continue testing the glass-Si packages in-vitro. Tests will also continue on electroplate gold films with a sputtered SiO_2 dielectric spacer. Furthermore, active probes with this technology will be fabricated for use in chronic in-vivo implants. Finally, the redesigned FINESS chip will be fabricated and tested in the coming quarter.